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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is a thing to carry out concerning the suitable aging approach especially for DC mold plasma display, and aging equipment about the aging approach of a display and aging equipment equipped with two or more display cels.
[0002]
[Description of the Prior Art] Drawing 15 is structural drawing of DC mold plasma display (it is also hereafter called a panel also with PDP again). On the tooth-back substrate 201 of glass, thick film screen printing forms the display anode plate 202, the auxiliary anode 203, the display anode plate lead 204, and the auxiliary anode lead 205. Moreover, resistance 206 is formed between the display anode plate 202 and the display anode plate lead 205 and between the auxiliary anode 203 and the auxiliary anode lead 205. A discharge current value can be small held down by this resistance 206, and reinforcement of a panel can be attained. Except for the parts of the display anode plate 202 on the tooth-back substrate 201, and an auxiliary anode 203, it insulates with a dielectric 207 and the obstruction 208 is printed on it. The discharge space of a cel is formed with this obstruction 208. There is an auxiliary cel 210 to two display cels 209, and, in the charged particle and metastable particle which were generated in the discharge in the auxiliary cel 210, close lowers breakdown voltage to the display cel 209 on either side. The fluorescent substance 211 is applied to the base except the side face and the display anode plate 202 of an obstruction 208 in the display cel 209. The display anode plate 202 and an auxiliary anode 203, and the cathode 213 run perpendicularly are formed in the front substrate 212.
[0003] It precedes for carrying out pattern display actuation (image display actuation) of the above-mentioned PDP, and the aging process (aging is only called hereafter) which drives PDP on specific actuation conditions is carried out. The object of an aging process is an improvement of the electrical characteristics of a cel electrically, and, chemically, an electrode etc. is washing on the front face of a cel. An ESHINGU process is carried out in front of a mercury diffusion process (mercury diffusion is only called hereafter) and in the back. Mercury diffusion is a process which heat is applied [process] to the quality of a solid by which the mercury which exists in a panel was added, mercury is steam-ized [process], and a long duration panel is further maintained [process] at an elevated temperature, and makes panel discharge space distribute mercury vapour uniformly. If mercury exists in a display cel, sputtering, such as cathode by the discharge gas which caused the life, will be eased, and the life of a panel will be prolonged.
[0004] If only aging before mercury diffusion has the large object which washes a cel front face and it washes the cel front face before mercury diffusion, the discharge voltage in early stages of after mercury diffusion (before aging after mercury diffusion) becomes the value of each cel proper, and it does not depend for it on the actuation conditions of aging before mercury diffusion. Moreover, aging after mercury diffusion has the large object which the discharge voltage of a cel reduces.
[0005] When a cel is driven, the discharge current which flows between the anode plate-cathode of a cel is called a cel current, and discharge voltage is called a cel electrical potential difference. In addition, the cel electrical potential difference (discharge voltage) in PDP includes the voltage drop in the resistance prepared in the anode plate of a cel. Moreover, actuation of the cel in aging is called aging actuation in distinction from pattern display actuation. The above-mentioned aging actuation is constant current

actuation which passes a fixed cel current in each cel. On the other hand, generally pattern display actuation is a constant voltage drive which impresses a fixed cel electrical potential difference to the display cel made to turn on.

[0006] Since it carries out by aging carrying out simple sequential scanning of the cathode line, and carrying out sequential actuation of each display cel and each auxiliary cel of PDP, if its attention is paid to one cel, in the cel, the turned-on period and the period which has not been turned on will be repeated by turns. The time amount (period) from initiation of the repeat of burning and an astigmatism LGT to termination is called aging time amount (aging period). Moreover, in an aging period, the sum total of the burning time amount of one cel is called aging-on time amount, and the rate of aging-on time amount to aging time amount is called on-duty. When the period which scans an one-line scan period and all cathode lines for the period which scans 1 cathode line of PDP here was made into the one-frame scan period and its attention is paid to one cel, the turned-on period is equal to an one-line scan period, and is equal to an one-frame scan period. [of the period from burning to the next burning]

[0007] Drawing 16 is the block diagram showing the configuration of conventional aging equipment. The aging equipment shown in drawing 16 has the display anode plate current regulator circuit 101, the display anode plate driver circuit 2, the auxiliary anode current regulator circuit 3, the auxiliary anode driver circuit 4, and the cathode driver circuit 5 and a signal generating circuit 106, and ages PDP7. The display cel constant current signal 111 common to all display cels is inputted into the anode plate driver circuit 103 from the display anode plate current regulator circuit 101, and the auxiliary cel constant current signal 27 common to all auxiliary cels is inputted into the auxiliary anode driver circuit 4 from the auxiliary anode current regulator circuit 3. The display anode plate driver circuit 2 has the display anode plate output terminal 25 of the number of display anode plate lines and the same number of PDP7. Each display anode plate output terminal 25 is connected according to an individual on the corresponding display anode plate line. This display anode plate driver circuit 2 impresses a forward electrical potential difference to all the display anode plate lines of PDP7. The auxiliary anode driver circuit 4 has the auxiliary anode output terminal 26 of the number of auxiliary anode lines and the same number of PDP7. Each auxiliary anode output terminal 26 is connected according to an individual on the corresponding auxiliary anode line. This auxiliary anode driver circuit 4 impresses a forward electrical potential difference to all auxiliary anode lines. Moreover, the cathode driver circuit 5 has the cathode output terminal 24 of the number of cathode lines and the same number of PDP7. Each cathode output terminal 24 is connected according to an individual on the corresponding cathode line. This cathode driver circuit 5 makes sequential selection of the one cathode line of PDP7 for every one-line scan period based on the scan pulse 16 and the shift clock 15 which are inputted from a signal generating circuit 106, and connects it to a touch-down power source (other cathode lines which were not chosen serve as floating). In addition, the internal configuration of the display anode plate current regulator circuit 101 and the auxiliary anode current regulator circuit 3 is the same, and only calls these an anode plate current regulator circuit. Moreover, except that the numbers of anode plate lines used as the object for actuation differ (one auxiliary anode line is prepared to two display anode plate lines), the internal configuration of the display anode plate driver circuit 2 and the auxiliary anode driver circuit 4 is the same, and only calls these an anode plate driver circuit.

[0008] Drawing 17 is the circuit diagram showing the configuration of the anode plate current regulator circuit (101 and 3) of drawing 16 , and an anode plate driver circuit (2 and 4). The anode plate current regulator circuit 108 has the NPN mold transistor Tr1 and the PNP mold transistor Tr2 by which Darlington connection was carried out, protective resistance R1 and R2, and the variable resistance Rv for volumes. variable resistance Rv has the 1st lock-pin connected to the positive supply Va, the 2nd lock-pin connected to power-source Va-10 (a power source Va -- 10 [V] -- low), and the adjustable pin connected to the base electrode of the current monitor section and a transistor Tr1. The emitter electrode of a transistor Tr1 is connected to power-source Va-10 through resistance R1, and the collector electrode of Tr1 is connected to the power source Va. the base electrode of a transistor Tr2 is connected to the emitter electrode of a transistor Tr1, the emitter electrode of Tr2 is connected to a power source Va through resistance R2, and the collector electrode of Tr2 is connected to power-source Va-5 (a power source Va -- 5 [V] -- low). The emitter electrode of Tr2 serves as an output terminal of the constant current signal 113 (the display cel constant current signal 111 or the auxiliary cel constant current signal 27 of drawing 16).

[0009] Moreover, as for the anode plate driver circuit 109, only the number of display anode plate lines or the number of auxiliary anode lines, and the same number have the driver unit which serves as protective resistance R4 and R5 and the transistor Tr4 for constant current from the anode plate output terminal 110 (the display anode plate output terminal 25 or auxiliary anode output terminal 26). The constant current signal 113 is inputted into the base electrode of a transistor Tr4, the emitter electrode of Tr4 is connected to a power source Va through resistance R4, and the collector electrode of Tr4 is connected to the anode plate output terminal 110 through resistance R5. Each anode plate output terminal 110 is connected to the anode plate line (a display anode plate line or auxiliary anode line) on which PDP7 corresponds.
[0010] In the anode plate current regulator circuit 108 and the anode plate driver circuit 109, when bias of the base electrode of a transistor Tr1 is carried out to power-source Va-10 by the adjustable pin of variable resistance Rv, transistors Tr1, Tr2, and Tr4 are turned off, and since a forward electrical potential difference is not impressed to the anode plate line of PDP7, a cel current does not flow. If the adjustable pin of variable resistance Rv is moved to a power-source Va side and the base potential of a transistor Tr1 is raised, transistors Tr1, Tr2, and Tr4 turn on, and if a power source Va is more than the electrical potential difference (about 300 [V]) of a cel that can be discharged In the cel linked to one cathode line chosen by the cathode driver circuit 5 (refer to drawing 16), a cel current flows through a transistor Tr4, the anode plate output terminal 110, and the anode plate line of PDP7. If the base potential of a transistor Tr1 is furthermore raised, the current and voltage level of the constant current signal 113 will go up, and, thereby, a cel current will become large gradually. In addition, the set point of a cel current is displayed on the current monitor section.
[0011] In drawing 16 and the conventional aging equipment of drawing 17 , a cel current is set as 30-100 [muA]. Moreover, in an one-frame scan period, one-line scan period [every] aging actuation of each cel is carried out. An one-line scan period is set as 500[mus] -5[ms]. In conventional aging equipment, the aging time amount, aging-on time amount, and on-duty of all cels are common. For example, when the number of cathode lines is 256, on-duty becomes 1/256. When on-duty is 1/256, aging time amount is set up in 3 - 5 hours.
[0012]
[Problem(s) to be Solved by the Invention] The cel current-cel voltage characteristic (an I-V property is called hereafter) of the cel in early stages of after mercury diffusion is decided by the cel configuration and the value of resistance prepared in the display anode plate, and dispersion is in the same panel between cels. Moreover, the I-V property of all cels shifts from the property in early stages of after mercury diffusion only the almost same amount as the direction which lowers a cel electrical potential difference depending on aging-on time amount according to aging after mercury diffusion (the cel electrical potential difference when carrying out constant current actuation falls uniformly). In the above-mentioned conventional aging, since all the display cels contained in one panel are aged on the same conditions, even if aging after mercury diffusion is completed, I-V property dispersion between cels exists.
[0013] If big dispersion is in the I-V property of the display cel in a panel, big dispersion will appear in a cel current (discharge current) at the time of constant voltage drives, such as pattern display actuation. If it exists in the place which is not filled within limits which cause incorrect burning and have been seen from the average if it exists in the place beyond within the limits as which the cel current value at the time of a constant voltage drive is regarded from the average, it will become the factor of a non-LGT cel. That is, if dispersion in an I-V property (especially cel current) is large, the pattern display quality of the panel will deteriorate.
[0014] It is made in order that this invention may solve such a conventional technical problem, and it aims at offering the aging approach of a display and aging equipment which can amend I-V property (especially cel current) dispersion between display cels.
[0015]
[Means for Solving the Problem] In order to attain the above-mentioned object, the aging approach of the display of this invention is characterized by including the process which sets up the aging-on time amount of each display cel according to an individual, and the process at which only the aging-on time amount set up according to the individual carries out aging actuation of each display cel.
[0016] Moreover, the aging equipment of the display of this invention is characterized by having a

storage means to memorize the cell data of each display cel, and an aging means by which only the aging-on time amount according to individual according to said cell data carries out aging actuation of each display cel.

[0017]

[Embodiment of the Invention] Gestalt 1 drawing 1 of operation is the block diagram showing the configuration of the PDP aging equipment of the gestalt 1 of operation of this invention. The aging equipment of drawing 1 has the display anode plate current regulator circuit 1, the display anode plate driver circuit 2, the auxiliary anode current regulator circuit 3, the auxiliary anode driver circuit 4, and the cathode driver circuit 5 and a digital disposal circuit 6, and ages PDP7. Moreover, drawing 2 is the circuit diagram showing the configuration of the PDP aging equipment of the gestalt 1 of operation of this invention. In addition, in drawing 2 , since the internal configuration of the auxiliary anode current regulator circuit 3 and the auxiliary anode driver circuit 4 is the same as usual, a graphic display and explanation of an internal configuration are omitted.

[0018] The number of display cels is DC mold plasma display of a mxn (m is forward integer and n is forward even number) individual, and PDP7 has m cathode lines, n display anode plate lines (display anode plate lead), and n/2 auxiliary anode line (auxiliary anode lead). In addition, ALj [KLi and the j-th (j is integer of arbitration from 1 to n) display anode plate line] is written for the i-th (i is integer of arbitration from 1 to m) cathode line. Moreover, it writes CE [the display cel by the cathode line KLi and the display anode plate line ALj] (i, j). Here, it shall be m=n=256.

[0019] A digital disposal circuit 6 has the basic signal generating circuit 61, the address signal generating circuit 62, a timer circuit 63, latch circuits 64 and 68, memory 65, a comparison circuit 66, and a shift register circuit 67. The basic signal generating circuit 61 generates the address basic signal 10, the read-out enable signal 11, the timer count basic signal 12, the shift clock 13, the latch clock 14, the scan shift clock 15, and the scan pulse 16. Moreover, the address signal generating circuit 62 generates an address signal 17 based on the inputted address basic signal 10, and outputs this to memory 65. In addition, the timer count basic signal 12 should just turn into a basic signal of the elapsed time data signal 18 generated by the timer circuit 63 that the address basic signal 10 should just be a thing used as the basic signal of an address signal 17.

[0020] A timer circuit 63 generates the elapsed time data in which the elapsed time from aging initiation is shown based on the timer count basic signal 12 inputted from the basic signal generating circuit 61, and outputs the elapsed time data signal 18. The elapsed time data of the elapsed time data signal 18 are updated with 1/16 of the periods of an one-line scan period here. Moreover, a latch circuit 64 latches the elapsed time data signal 18 for every standup of the latch clock 14, and outputs the latched data as an elapsed time maintenance data signal 20. The elapsed time maintenance data signal 20 is updated for every one-line scan period here. An one-line scan period is a period from the standup of the scan shift clock 15 or the latch clock 14 to the next standup.

[0021] Memory 65 outputs the cell data memorized to the address specified by the address signal 17 as a cell-data signal, when the cell data is memorized and data read-out actuation is permitted by the read-out enable signal 11.

[0022] A cell data shall be data in which the aging-on time amount set up according to the individual for every display cel is shown, and shall be 8 bit data here. With the gestalt 1 of this operation, aging of a display cel is carried out by common on-duty, and a cell data is data in which the aging time amount according to individual of each display cel is shown. Here, since aging is carried out by sequential scanning of a cathode line, if its attention is paid to one display cel, in the display cel, the turned-on period and the period which has not been turned on will be repeated by turns. Aging time amount (period) shows the time amount (period) from initiation of the repeat of burning and an astigmatism LGT to termination. Moreover, aging-on time amount shows the sum total of the burning time amount of 1 display cel in an aging period, and on-duty shows the rate of aging-on time amount to aging time amount. In the aging equipment of the gestalt 1 of this operation, although initiation of an aging period is in agreement with aging initiation of PDP7, termination of an aging period differs for every display cel according to a cell data.

[0023] From memory 65, reading appearance of the cell data of 256 display cels belonging to one cathode line is carried out to an one-line scan period. That is, the cell data of 256 display cels CE (i, 1)-CE (i, 256) linked to the cathode line KLi is read from memory 65 to the scan period of the cathode line

KL (i-1). although the cell data from memory 65 carries out reading appearance and the gestalt is arbitrary, the cell data of the 256 above-mentioned display cels shall be read to an one-line scan period here by making the single address period of memory 65 into 1/16 of one-line scan periods, and carrying out reading appearance of the cell data of 16 display cels to a single address period simultaneously (to parallel), and reading 16 cell datas to 16 address period one by one (serial)

[0024] Therefore, memory 65 shall be equipped with 16 8-bit buses here, shall have memorized 16x8-bit data (16 cell datas) to the single address, and shall output this 16 cell data to 16 above-mentioned buses as 16 cell-data signals 19-1 to 19-16, respectively. Moreover, the display anode plate lines AL1-AL256 of PDP7 shall be divided into 16 display anode plate line groups, and the cell data of 16 display cels which belong to the same cathode line and belong to the same display anode plate line group shall be memorized in the single address of memory 65. They are the 16 above-mentioned display anode plate line groups ALG1 and ALG2 -- It is written as ALG16. Here, the display anode plate lines AL1-AL16 shall constitute the display anode plate line group ALG 1, AL17-AL32 shall constitute ALG2, ALG3-ALG15 shall be constituted like the following, and AL241-AL256 shall constitute ALG16.

[0025] A comparison circuit 66 generates the elapsed time maintenance data of the elapsed time maintenance data signal 20, and the 1-bit comparison result data which become off when the size of cell-data signal 19-k (k is the integer of the arbitration to 1-16) is compared, elapsed time maintenance data are below a cell data, and ON and elapsed time maintenance data are larger than a cell data, and outputs them as comparison result data signal 21-k. 16 comparison result data are generated at a time respectively corresponding to 16 cell datas of the cell-data signal 19-1 to 19-16 for 1/16 of every periods of an one-line scan period, and are outputted as 16 comparison result data signals 21-1 to 21-16, respectively. Moreover, comparison result data signal 21-k contains 16 comparison result data corresponding to 16 display cels at 1 scan-line period, respectively.

[0026] A shift register circuit 67 has 16 shift registers into which the comparison result data signal 21-1 to 21-16 is inputted into, respectively, and the shift clock 13 is inputted in common. Shift registers are 16 steps of shift registers which consist of 16 bit registers, and carry out the sequential shift of the comparison result data of comparison result data signal 21-k in the standup of the shift clock 13. The shift clock 13 is a clock of 1/16 period of an one-line scan period. This shift register circuit 67 changes into parallel data 256 comparison result data contained in the comparison result data signal 21-1 to 21-16 at an one-line scan period, and outputs this 256 comparison result data to a latch circuit 68 from the output terminal of 256 bit registers of the 16 above-mentioned shift registers. Moreover, a latch circuit 68 latches 256 comparison result data corresponding to 256 display cels which belong to the cathode line scanned from now on, and belong to all display anode plate lines with the latch clock 14, and outputs the latched data to the display anode plate current regulator circuit 1 as an aging control signal 22-1 to 22-256 of the 256 above-mentioned display cels.

[0027] The display anode plate current regulator circuit 1 has display anode plate line several n of the variable resistance Rv and PDP7 for volumes, and the display anode plate constant current unit of the same number. variable resistance Rv with the 1st lock-pin connected to the positive supply Va, and the 2nd lock-pin connected to power-source Va-10 (a power source Va -- 10 [V] -- low) The aging control signal 22-1 to 22-256 which has the adjustable pin connected to the current monitor section and all constant current units, and was inputted from the digital disposal circuit 1, Based on setting out of the adjustable pin of variable resistance Rv, the constant current signal 23-1 to 23-256 is generated, and this is outputted to the display anode plate driver circuit 2.

[0028] Each display anode plate constant current unit is constituted by the NPN mold bipolar transistor Tr1, the PNP mold bipolar transistor Tr2, the P channel field-effect transistor Tr3, and protective resistance R1 and R2, and generates constant current signal 23-j based on inputted aging control signal 22-j and setting out of the adjustable pin of variable resistance Rv. The base electrode of a transistor Tr1 is connected to the adjustable pin of variable resistance Rv, an emitter electrode is connected to power-source Va-10 through resistance R1, and the collector electrode is connected to the power source Va. The base electrode of a transistor Tr2 is connected to the emitter electrode of a transistor Tr1, the emitter electrode of Tr2 is connected to a power source Va through resistance R2, and the collector electrode of Tr2 is connected to power-source Va-5. The emitter electrode of a transistor Tr2 serves as an output terminal of constant current signal 23-j. Aging control signal 22-j is inputted into the gate electrode of a transistor Tr3 from a digital disposal circuit 6, the source electrode of Tr3 is connected to a power

source Va, and the drain electrode is connected to the emitter electrode of a transistor Tr1, and the base electrode of a transistor Tr2.

[0029] The display anode plate driver circuit 2 has the display anode plate driver unit of display anode plate line several n of PDP7, and the same number as usual. Each display anode plate driver unit is constituted by the current-limiting resistance R4 and R5, a transistor Tr4, and display anode plate output terminal 25-j. Constant current signal 23-j is inputted into the base electrode of a transistor Tr4 from the constant current unit with which the display anode plate current regulator circuit 1 corresponds, and the emitter electrode of Tr4 is connected to a power source Va through resistance R4, and the collector electrode is connected to display anode plate output terminal 25-j through resistance R5. Display anode plate output terminal 25-j is connected to the display anode plate line on which PDP7 corresponds.

[0030] The cathode driver circuit 5 is the same configuration as the former, and has the shift register 51 of the same number of stages as cathode line several m of PDP7, and cathode line several m and the cathode driver unit of the same number. Each cathode driver unit is constituted by the P channel field-effect transistor Tr5 and cathode output terminal 24-i. A shift register 51 has the clock input terminal into which the scan shift clock 15 is inputted from a digital disposal circuit 6, the data input terminal into which the scan pulse 16 is inputted from a digital disposal circuit 6, the bit register of the number of cathode lines and the same number of PDP7, and the output terminal (output terminal of each bit register) of the number of cathode lines and the same number of PDP7, and carries out the sequential shift of the scan pulse 16 for every standup of the scan shift clock 15. Moreover, a transistor Tr5 is a transistor for cathode scan switching, the gate electrode of Tr5 is connected to the output terminal to which a shift register 51 corresponds, and a drain electrode is connected to cathode output terminal 24-i, and the source electrode is connected to the touch-down power source. Cathode output terminal 24-i is connected to the cathode line on which PDP7 corresponds.

[0031] In addition, the memory 65 of a digital disposal circuit 6 constitutes a storage means to memorize the cell data of each display cel. Moreover, the digital disposal circuit 6 except memory 65, the display anode plate current regulator circuit 1, the display anode plate driver circuit 2, and the cathode driver circuit 5 constitute the aging means which carries out aging actuation of each display cel from common on-duty until the aging time amount according to individual according to a cell data passes. Moreover, the timer circuit 63 of a digital disposal circuit 6 constitutes a timer means to generate the elapsed time data in which the elapsed time from aging initiation is shown. A comparison circuit 66, a shift register circuit 67, and a latch circuit 68 By comparing a cell data with elapsed time data, it judges whether it went through the aging time amount set up according to the individual, and the control means which generates the aging control signal which shows whether aging actuation is carried out based on this judgment result or it does not carry out for every display cel is constituted. Moreover, the display anode plate current regulator circuit 1 and the display anode plate driver circuit 2 constitute the driving means which carries out aging actuation of each display cel according to an individual based on an aging control signal.

[0032] Next, actuation of the PDP aging equipment of drawing 1 is explained. Drawing 3 is the actuation timing chart of the PDP aging equipment of the gestalt 1 of operation. In drawing 3 , an address signal 17-1 and 17-2 (17-1 is the high order bit data of an address signal 17, and 17-2 is the low order bit data of 17), The read-out enable signal 11 and the cell-data signal 19-1 to 19-16 (19-3 to 19-15 is a graphic display abbreviation), The elapsed time data signal 18, the elapsed time maintenance data signal 20, and the latch clock 14, The shift clock 13 and the comparison result data signal 21-1 to 21-16 (21-3 to 21-15 is a graphic display abbreviation), Each timing chart of cathode output terminal 24-1 - 24 -256 (24-2 to 24-255 is a graphic display abbreviation) electrical potential difference is indicated to be the aging control signal 22-1 to 22-256 (for 22-3 to 22-255 to be a graphic display abbreviation), the scan shift clock 15, and the scan pulse 16.

[0033] An address signal 17-1 is a 8-bit signal which specifies the address of 256 display cels CE belonging to the cathode line KLi (i, 1) - (i, 256) a cell data. KL1 grade written to the address signal 17-1 of drawing 3 shows the cathode line then specified. Moreover, an address signal 17-2 is a 4-bit signal which specifies the address of the cell data of 16 display cels which serve as low order bit data of an address signal 17-1, and belong to the 256 above-mentioned display cel CE (i, 1) - (i, 256) inside, and display anode plate line group ALGk. The number written to the address signal 17-2 of drawing 3 shows the number of the display anode plate line group then specified (for example, "1" shows the display

anode plate line group ALG 1). moreover -- reading -- appearance -- carrying out -- an enable signal -- 11 -- memory -- 65 -- data output -- actuation -- authorization -- /-- prohibition -- deciding -- a signal -- it is -- drawing 3 -- **** -- aging -- equipment -- operating -- **** -- between -- always -- data output -- actuation -- authorization -- being shown -- " -- H" -- level -- becoming -- a signal -- it is .

[0034] Memory 65 outputs simultaneously the cell data of 16 display cels belonging to the cathode line specified by total of the 12-bit address signal 17, and an anode plate line group as a cell-data signal 19-1 to 19-16, respectively. The number written to the cell-data signal 19-1 to 19-16 of drawing 3 shows the number of the display anode plate line where the display cel corresponding to the data belongs (for example, "256" shows the display anode plate line AL256).

[0035] By counting up the timer count basic signal 12, a timer circuit 63 generates 8-bit elapsed time data (the number of bits of elapsed time data is made equal to the number of bits of a cell data), and outputs this elapsed time data as an elapsed time data signal 18. The elapsed time data signal 18 is updated for 1/16 of every periods of an one-line scan period. Moreover, by latching the data of the elapsed time data signal 18 in the standup of the latch clock 14, a latch circuit 64 generates 8-bit elapsed time maintenance data, and outputs this elapsed time maintenance data as an elapsed time maintenance data signal 20. The elapsed time maintenance data signal 20 is updated for every period from the standup of the latch clock 14 to the next standup, i.e., an one-line scan period.

[0036] A comparison circuit 66 compares the size of the time maintenance data of the elapsed time maintenance data signal 20, and the cell data of cell-data signal 19-k (k is the integer of the arbitration from 1 to 16), when elapsed time maintenance data are below a cell data, and ON and elapsed time maintenance data are larger than a cell data, it generates the 1-bit comparison result data which become off, and it outputs them as a comparison result data signal 21-1 to 21-16. That is, by comparing with elapsed time data the cell data which shows the aging-on time amount of the display cel set up according to the individual, a comparison circuit 66 judges whether aging-on time amount passed, and when aging-on time amount has not passed, and it has turned on and has passed, it generates the 1-bit comparison result data which become off. it is shown that the comparison result data of ON continue aging (ON / off repeat of aging actuation) of a corresponding display cel, and off comparison result data end aging (ON / off repeat of aging actuation) of a corresponding display cel -- it is -- it is -- not carrying out is shown. The number written to the comparison result data signal 21-1 to 21-16 of drawing 3 shows the number of the display anode plate line where the display cel corresponding to the data belongs (for example, "256" shows the display anode plate line AL256). The comparison result data signal 21-1 to 21-16 is updated for 1/16 of every periods of an one-line scan period.

[0037] By carrying out the sequential shift of the comparison result data of the comparison result data signal 21-1 to 21-16 in the standup of the shift clock 13 in each 16 shift register, a shift register circuit 67 changes 256 comparison result data corresponding to the display cels CE (i, 1)-CE (i, 256) into parallel data in an one-line scan period, respectively, and outputs this to a latch circuit 68.

[0038] A latch circuit 68 latches the 256 above-mentioned comparison result data in the standup of the latch clock 14, and outputs the aging control signal 22-1 to 22-256 of the display cels CE (i, 1)-CE (i, 256) for the latched data. Aging control signal 2-j is inputted into the j-th display anode plate constant current unit of the display anode plate current regulator circuit 1. The number written to the aging control signal 22-1 to 22-256 of drawing 3 shows the number of the display cel corresponding to the signal period (for example, "" (256 1) shows the display cel CE belonging to the cathode line KL256 (256 1), and "" (1 1) shows the display cel CE belonging to the cathode line KL1 (1 1)). The level of the aging control signal 22-1 to 22-256 is updated for every one-line scan period. Here, when the comparison result data which an aging control signal serves as "H" level (power-source Va level), and correspond when corresponding comparison result data are ON are OFF, an aging control signal shall serve as "L" level.

[0039] When aging control signal 22-j is "H" level, in the j-th constant current unit of the display anode plate current regulator circuit 1, a transistor Tr3 is still OFF, to transistors Tr1 and Tr2, the current between emitter-collectors according to setting out of variable resistance Rv flows, and constant current signal 23-j according to the current between emitter-collectors of a transistor Tr2 is outputted to the j-th display anode plate driver unit of the display anode plate driver circuit 2. In the j-th driver unit of the display anode plate driver circuit 2, the current between emitter collectors according to constant current signal 23-j flows to a transistor Tr4. This current is supplied to the display anode plate line ALj through

resistance R4 and display anode plate output terminal 25-j, and turns into the discharge current of the display cel CE (i, j). That is, when aging control signal 22-j is "H" level, in the one-line scan period when the corresponding cathode line KLi is chosen by the cathode driver circuit 5, aging actuation of the display cel CE (i, j) is carried out.

[0040] On the other hand, since a transistor Tr3 turns on, the base electrode of a transistor Tr2 serves as power-source Va level by this in the j-th constant current unit of the display anode plate current regulator circuit 1 and Tr2 turns off when aging control signal 22-j is "L" level, constant current signal 23-j is set to power-source Va level. Since constant current signal 23-j is power-source Va level, the transistor Tr4 of the j-th driver unit of the display anode plate driver circuit 2 is turned off, the display anode plate line ALj serves as floating by this, and the discharge current does not flow in the display cel CE (i, j). That is, when aging control signal 22-j is "L" level, even if the corresponding cathode line KLi is chosen by the cathode driver circuit 5, aging actuation of the display cel CE (i, j) is not carried out.

[0041] Actuation of the cathode driver circuit 5 is the same as the former, and the scan pulse 16 carries out the sequential shift of the 256 bit registers of a shift register 51 synchronizing with the standup of the scan shift clock 15. In an one-line scan period (= the period from the standup of the scan shift clock 15 to the next standup), only the output of the bit register holding the scan pulse 16 serves as forward potential, the transistor Tr5 corresponding to this bit register turns on, and one cathode output terminal 24 corresponding to this Tr5 serves as touch-down potential (GND). Moreover, all of the output of other bit registers which do not hold the scan pulse 16 become touch-down potential, 255 transistors Tr5 corresponding to these bit registers are having turned all off with as, and 255 cathode output terminals 24 corresponding to these Tr(s)5 serve as high impedance. That is, the cathode line linked to the cathode output terminal 24 which the cathode output terminal 24-1 to 24-256 became sequential touch-down potential alternatively for every one-line scan period, and became touch-down potential is chosen. The cathode line KLi is chosen when cathode output terminal 24-i becomes touch-down potential, and aging actuation only of the display cel which has not reached the setting-out aging time amount the elapsed time after starting aging among the display cels CE (i, 1)-CE (i, 256) belonging to the cathode line KLi is indicated to be to a cell data is carried out selectively.

[0042] Here, electrical property change of the display cel by the electrical characteristics of the display cel in early stages of after mercury diffusion and aging after mercury diffusion is explained. In addition, in the following explanation, a "cel current" shall show the discharge current which flows between the display anode plate-cathode of a display cel, when a display cel is driven, and a "cel electrical potential difference" shall show the discharge voltage when driving a display cel. Moreover, "aging" shall show aging after mercury diffusion. The cathode of a display cel is connected to the cathode line, and the display anode plate is connected to the display anode plate line through resistance. The cathode line KLi is connected to cathode output terminal 24-i of the cathode driver circuit 5, and the anode plate line ALj is connected to display anode plate output terminal 25-j to which the display anode plate driver circuit 2 corresponds. Including the voltage drop in resistance of the above [a cel electrical potential difference], if the cathode line KLi is scanned, cathode will serve as touch-down potential. Therefore, what is necessary is just to measure the potential of display anode plate output terminal 25-i, in order to survey the cel electrical potential difference of the display cel CE (i, j). Moreover, what is necessary is just to measure the current which flows to display anode plate output terminal 25-j, in order to survey the cel current of the display cel CE (i, j).

[0043] Drawing 4 is drawing which plotted the cel electrical potential difference of all the display cels contained on 1 display anode plate line of the arbitration when carrying out constant current actuation of the panel in early stages of after mercury diffusion (before aging) in order of the scan. The case where a cel current is set as the case where it is set as 30 [muA], and 50 [muA] is shown in drawing 4 . Moreover, the panel with 256 cathode lines (inside, three dummy cathode lines) was used. The number of display cels used as the measuring object of a cel electrical potential difference is 256 pieces. The cel numbers 1-256 have shown 256 display cels to drawing 4 .

[0044] The cel current-cel voltage characteristic (I-V property) of a display cel can be expressed as V=z (I)+v0 using the cel current I, and the cel electrical potential difference V, and function [of the cel current I] z (I) and functions v0 other than the cel current I. The differential of z (I) which is the inclination of an I-V property is called a SERUPI dance, and v0 which is a cel electrical potential difference at the time of the cel current I= 0 is called a cel electrical-potential-difference intercept (cel V

intercept). Drawing 5 is drawing which plotted the cel impedance of the display cel shown in drawing 4 in order of the scan. Moreover, drawing 6 is drawing which plotted V intercept of the display cel shown in drawing 4 in order of the scan. It asks for the cel impedance of drawing 5 , and the cel V intercept of drawing 6 by primary approximation using drawing 4 . That is, primary approximation property V=ZxI+V0 (Z and V0 are a constant) of an I-V property was calculated using the actual measurement (the cel current 30 [muA] and cel electrical potential difference to 50 [muA]) of two pieces in the display cel of the number of the arbitration of drawing 4 , and inclination Z of this primary approximation property was considered as the SERUPI dance, and V0 which is a cel electrical potential difference at the time of the cel current I= 0 was used as the cel V intercept.

[0045] Drawing 7 is drawing which plotted the cel current when carrying out the constant voltage drive of the display cel shown in drawing 4 in order of the scan. A cel electrical potential difference is set as the average electrical-potential-difference value for example, at the time of pattern display actuation. The cel electrical-potential-difference value was set to 248 [V] in drawing 7 . Moreover, in drawing 7 , the cel current value was calculated by count. That is, the cel current I was calculated by setting the cel electrical potential difference V to above 248 [V], and making the cel impedance Z into the value of drawing 5 using primary approximation property I=(V-V0)/Z of an I-V property, and making the cel V intercept V0 into the value of drawing 6 . Moreover, drawing 8 is the histogram of the cel current of drawing 7 . For the display cel of 25-30 [muA], as for 118 pieces and the display cel of 40-45 [muA], in drawing 8 , the number of 12 pieces and the display cels of 35-40 [muA] of 121 pieces and the display cel of 45-50 [muA] is [a cel current value / the cel of one piece, and 30-35 [muA]] one.

[0046] In the panel in early stages of after mercury diffusion, as shown in drawing 5 and drawing 6 , dispersion is in the I-V property (a cel V intercept and cel impedance) of a display cel, therefore there is dispersion as shown in drawing 7 and drawing 8 in the cel current at the time of a constant voltage drive. Since pattern display actuation of a panel is a constant voltage drive which usually impresses a fixed cel electrical potential difference (write-in electrical potential difference) to the display cel made to turn on, there is dispersion as shown in drawing 7 and drawing 8 in the cel current at the time of pattern display actuation.

[0047] Next, although especially a cel impedance will not change if it ages to the panel in early stages of after mercury diffusion, a cel V intercept falls with aging-on time amount. The decrement of a cel V intercept is mainly decided by aging-on time amount, and does not vary for every display cel. In addition, in aging, by transmission lowering of the front plate by adhesion of a spatter object, although the brightness of a display cel falls with aging time amount, the rate of change of brightness does not influence display quality so much small, either.

[0048] Drawing 9 is drawing showing the drop property of a cel V intercept over the aging time amount in the display cel of arbitration. The average in two or more display cels extracted from two or more PDP(s) is shown in drawing 9 . Moreover, the case where a cel current is set as the case where it is set as 100 [muA], and 200 [muA] is shown. Moreover, the on-duty of aging is 1/256 (therefore, aging-on time amount becomes 1/256 of ESHINGU time amount). Moreover, change of a cel V intercept has shown the cel V intercept in early stages of [after mercury diffusion] mercury (= aging time amount 0 minute) as criteria (0 [V]).

[0049] As shown in drawing 4 thru/or drawing 7 , there is dispersion in the I-V property (a cel V intercept and cel INI dance) of the display cel in the panel in early stages of after mercury diffusion. If it ages, the cel V intercept of all display cels becomes small, and a cel impedance will be before and after aging, and will hardly change. The decrement of the cel V intercept of a display cel is decided by aging only depending on aging-on time amount, and it is not dependent on the value of the cel V intercept before aging (early stages of mercury diffusion). Therefore, when only the same time amount carries out aging actuation of all the display cels, the reduction variation of the cel V intercept of all display cels becomes the same. namely, when aging which made the same aging-on time amount of all display cels like before is carried out Although an I-V property shifts only a constant rate to cel V intercept shaft orientation and the cel current of all the display cels at the time of a constant voltage drive becomes large by this since, as for the cel V intercept of all display cels, only a constant rate becomes small and a cel impedance does not change Dispersion in the cel current between display cels still exists. From the above thing, in order to suppress dispersion in the cel current at the time of a constant voltage drive In the panel before aging, an I-V property (specifically good in a primary approximation property) is

searched for by location survey for every display cel. The decrement of a cel V intercept required in order to make the cel current at the time of constant current actuation increase to reference current is calculated based on the above-mentioned I-V property. What is necessary is to convert the need decrement of this cel V intercept into aging time amount with the change property of a cel V intercept over the aging time amount of drawing 9 , and just to age each display cel by the aging time amount according to the need decrement of a cel V intercept.

[0050] The aging approach of this invention does not carry out ESHINGU actuation of all the display cels by the same aging-on time amount like before. When the aging-on time amount of each display cel is set up according to an individual and only the set-up aging-on time amount carries out aging actuation of each display cel It is what is characterized by enabling it to amend dispersion in the cel current which adjusts the I-V property of a display cel according to an individual, and originates in dispersion in the I-V property of a display cel. The aging approach of the gestalt 1 this operation is characterized by aging by common on-duty (it being 1/256, when there are 256 cathode lines) until the aging time amount which the aging time amount of each display cel was set [time amount] up according to the individual, and had each display cel set up passes.

[0051] Below, the configuration procedure of the individual aging time amount of a display cel is explained. First, as explained in drawing 4 thru/or drawing 7 , two on the I-V property of each display cel are calculated by location survey, from these two points, the primary approximation property of an I-V property is calculated, and the cel impedance of drawing 5 , the cel V intercept of drawing 6 , and the cel current at the time of the constant voltage drive by the predetermined driver voltage of drawing 7 are searched for. At this time, a cel V intercept and a cel current may be searched for by location survey.

[0052] Next, reference current is set up. Reference current may be set up with reference to the cel current value or its dispersion degree of drawing 7 , and may be set up beforehand. Here, the cel current range 40-45 with most frequency [muA] is set up as reference current (for example, average of the current range) using the cel current frequency distribution shown in drawing 8 . However, although the cel current at the time of a constant voltage drive can be made to increase according to aging, since it cannot be made to decrease, the display cel of the cel current with which reference current is not filled is set as the object of the increment amendment in a cel current by aging, and the display cel of the cel current exceeding reference current becomes the outside of the object of cel current amendment according to aging. Therefore, it is necessary to set up reference current not only in consideration of frequency but in consideration of the number and its cel current of the display cel which becomes the outside of the object of amendment. In drawing 8 , one display cel of the cel currents 25-30 [muA], 12 display cels of 30-35 [muA], and 118 display cel [of 35-40 [muA]] ** are set as the object of cel current amendment, and one display cel of 45-50 [muA] becomes the outside of an object.

[0053] Next, the aging time amount of the display cel for amendment is set up based on the primary approximation property of drawing 5 thru/or the I-V property of drawing 7 , and the drop property of the cel V intercept of drawing 9 . The decrement of the cel V intercept corresponding to the difference of the cel current of the display cel for amendment and reference current is calculated based on the above-mentioned primary approximation property, and the aging time amount corresponding to the decrement of this cel V intercept is found from the drop property of a cel V intercept so that the cel current of the display cel for amendment may reach reference current. In the smaller display cel of a cel current, setting-out aging time amount becomes long. Moreover, as for the display cel more than reference current, a cel current sets setting-out aging time amount to 0 (it does not age). In drawing 8 , the aging time amount of the display cel below the cel current 40 [muA] is set up according to an individual, and the aging time amount of the display cel beyond the cel current 40 [muA] is set as 0.

[0054] Drawing 10 is drawing which plotted the setting-out aging time amount of drawing 4 thru/or the display cel of drawing 7 in order of the scan. The case where it is the case where a setting-out cel current is 100 [muA], and 200 [muA] is shown in drawing 10 . The display cel whose setting-out aging time amount is 0 minute is a display cel which does not age. In addition, although the display cel from which setting-out aging time amount becomes 1000 minutes or more is not plotted by drawing 10 , even if it carries out aging (1000 / 256-minute aging actuation) for 1000 minutes with the cel current 200 [muA], there is a display cel to which the cel current at the time of a constant voltage drive (at the time of the setting-out cel electrical potential difference 248 [V]) does not reach reference current in the panel used by drawing 4 thru/or drawing 8 actually. The cel which needs such ESHINGU of especially long time

amount (here above for 1000 minutes) usually processes as a defect panel to two or more cel **** case. In addition, when the cel which needs aging of long time amount is about 1-3 pieces, it may amend by the signal-processing approach.

[0055] Aging time amount is set up according to an individual for every display cel as mentioned above. Then, it ages by writing in the memory 65 (referring to drawing 2) of the aging equipment of the gestalt 1 of operation by making set-up aging time amount into a cell data.

[0056] Thus, since dispersion between display cels of the cel current at the time of a constant voltage drive can be amended by only the aging time amount according to individual aging each display cel of a panel, and having enabled it to adjust the I-V property of a display cel according to an individual according to the gestalt 1 of operation of this invention, a good pattern display without a non-LGT cel and an incorrect burning cel becomes possible.

[0057] The PDP aging equipment of the gestalt 2 of operation of gestalt 2 this invention of operation has the display anode plate current regulator circuit 1, the auxiliary anode current regulator circuit 2, the display anode plate driver circuit 3, the auxiliary anode driver circuit 4, the cathode driver circuit 5, and a digital disposal circuit 8. That is, let a digital disposal circuit 6 be a digital disposal circuit 8 in the PDP aging equipment of the gestalt 1 of the above-mentioned implementation. Drawing 11 is the circuit diagram showing the configuration of the PDP aging equipment of the gestalt 2 of operation of this invention. In addition, in drawing 11 , the same sign is given to the same thing as drawing 2 .

[0058] A digital disposal circuit 8 has the basic signal generating circuit 81, the address signal generating circuit 82, memory 83, and the Pulse-Density-Modulation circuit 84. The basic signal generating circuit 81 generates the address basic signal 30, the read-out enable signal 11, the pulse basic clock 32, the scan shift clock 15, and the scan pulse 16. Moreover, the address signal generating circuit 82 generates an address signal 35 based on the inputted address basic signal 30, and outputs this to memory 83. In addition, the address basic signal 30 should just turn into a basic signal of an address signal 35.

[0059] Memory 83 outputs the cell data memorized to the address specified by the address signal 35 as a cell-data signal, when the cell data is memorized and data read-out actuation is permitted by the read-out enable signal 11.

[0060] A cell data shall be data in which the aging-on time amount set up according to the individual for every display cel is shown, and shall be 8 bit data here. With the gestalt 2 of this operation, aging of a display cel is carried out by common aging time amount, and a cell data is data in which the on-duty according to individual of each display cel is shown. In the aging equipment of the gestalt 2 of this operation, the on-duty of each display cel of PDP7 is set as 1/256 or less value according to an individual.

[0061] Although the read-out gestalt of the cell data from memory 83 is arbitrary, the single address period of memory 83 is made into an one-line scan period, the aging time data of the 256 above-mentioned display cels shall be read to an one-line scan period, and the cell data of 256 display cels shall be simultaneously read to a single address period here. Therefore, memory 83 shall be equipped with 256 8-bit buses here, shall have memorized 256x8-bit data (256 cell datas) to the single address, and shall output this 256 cell data to 256 above-mentioned buses as 256 cell-data signals 36-1 to 36-256, respectively. Moreover, the cell data of 256 display cels belonging to the same cathode line shall be memorized in the single address of memory 83.

[0062] The Pulse-Density-Modulation circuit 84 is equipped with the counter circuit which counts the count of a standup (or falling) of the pulse basic clock 32, the latch circuit holding a cell data, etc., generates 256 pulses modulated by the width of face according to 256 cell datas of the cell-data signal 36-1 to 36-256, respectively, and outputs them to the display anode plate current regulator circuit 1 by making into the aging control signal 37-137 to 37-256 this 256 pulse by which width modulation was carried out, respectively. The pulse width of an aging control signal shows the on-duty of a corresponding display cel, and on-duty becomes large, so that width of face is wide. Since cell datas are 8 bit data, they can modulate pulse width to 256 steps (0 is included), and, thereby, can set the on-duty of a display cel as 256 steps. If the minimum value of a cell data is made to correspond to pulse width 0 and the maximum of a cell data is made to correspond to the pulse width of an one-line scan period (1/256 of periods of an one-frame scan period), the resolution of width modulation will become 1/255 of one-line scan periods. The minimum value of on-duty is set to 0, and maximum sets it 1/256. At this

time, the period of the Pulse-Density-Modulation basic clock 32 should just be 1/256 or less [of an one line scan period].

[0063] In addition, the memory 83 of a digital disposal circuit 8 constitutes a storage means to memorize the cell data of each display cel. Moreover, the aging means which carries out aging actuation of each display cel is constituted until aging time amount with the digital disposal circuit 8 except memory 83, the display anode plate current regulator circuit 1, the display anode plate driver circuit 2, and the cathode driver circuit 5 common to the on-duty according to individual according to a cell data passes. Moreover, the pulse-width-modulation circuit 84 of a digital disposal circuit 6 constitutes the control means which generates the aging control signal which shows the period which carries out aging actuation in a unit period (one-line scan period), and the period which does not carry out aging actuation for every display cel based on a cell data.

[0064] Next, actuation of the aging equipment of the gestalt 2 of operation is explained. Drawing 12 is the actuation timing chart of the PDP aging equipment of the gestalt 2 of operation. In drawing 12 , an address signal 35 and the read-out enable signal 11, The cell-data signal 36-1 to 36-256 (36-3 to 36-255 is a graphic display abbreviation), The pulse basic clock 32 and the aging control signal 37-1 to 37-256 (37-3 to 37-255 is a graphic display abbreviation), Each timing chart of cathode output terminal 24-1 - 24 -256 (24-2 to 24-255 is a graphic display abbreviation) electrical potential difference is indicated to be the scan shift clock 15 and the scan pulse 16.

[0065] An address signal 35 is a 8-bit signal which specifies the address of 256 display cels CE belonging to the cathode line KLi (i, 1) - (i, 256) a cell data. KL1 grade written to the address signal 35 of drawing 12 shows the cathode line then specified. In addition, if the number of bits of an address signal in case the number of a cathode line is m is set to q, it will be determined that it is set to 2q =m by number-of-bits q.

[0066] Memory 83 outputs simultaneously the cell data (8 bit data) of 256 display cels memorized to the address specified by the address signal 35 (it belongs to the cathode line specified by the address signal 35) to the Pulse-Density-Modulation circuit 84 as a cell-data signal 36-1 to 36-256, respectively. AL1 grade written to the cell data 36-1 to 36-256 of drawing 3 shows the display anode plate line where the display cel corresponding to the data belongs. Processing which outputs the cell data of 256 display cels belonging to the cathode line KLi to the Pulse-Density-Modulation circuit 84 is carried out at the scan period of the cathode line KL (i-1).

[0067] The pulse-width-modulation circuit 84 generates the pulse (WMP) by which width modulation was carried out to either of 256 steps of width of face to which the minimum width of face is made to 0, and it makes the maximum width an one-line scan period according to the cell data of cell-data signal 36-j, and outputs it to the constant current unit with which the display anode plate current regulator circuit 1 corresponds, using as aging control signal 37-j this pulse by which width modulation was carried out. The number written to the aging control signal 37-1 to 37-256 of drawing 12 shows the number of the display cel corresponding to the signal period (for example, "" (256 1) shows the display cel CE (256 1), and "" (1 1) shows the display cel CE (1 1)). The aging control signal 37-1 to 37-256 is updated for every one-line scan period. In addition, in the one-line scan period of the aging control signal 37-1 to 37-256, the period (period when an aging control signal serves as "H" level) when the pulse by which width modulation was carried out is located can be set as arbitration. Usually, although it may swerve from the standup of a pulse by which width modulation was carried out at the time of initiation of an one-line scan period, falling of a pulse may be arranged at the time of termination of an one-line scan period, and you may make it arrange the midpoint and pulse midpoint of one scan period.

[0068] The display anode plate current regulator circuit 1, the display anode plate driver circuit 2, the auxiliary anode current regulator circuit 3, the auxiliary anode driver circuit 4, and the cathode driver circuit 5 are the same as the gestalt 1 of the above-mentioned implementation. In the one line scan period when the cathode line KLi is chosen by the cathode driver circuit 5, a cel current is supplied only for the period which serves as "H" level by the pulse to which width modulation of the aging control signal 37-j was carried out to the display cel CE (i, j) by the display anode plate current regulator circuit 1 and the display anode plate driver circuit 2, and aging actuation of the display cel CE (i, j) is carried out only for the period when aging control signal 37-j is set to "H" level in the above-mentioned one-line scan period.

[0069] Drawing 13 is drawing showing the drop property of a cel V intercept over the aging-on duty

(pulse width of an aging control signal) in the display cel of arbitration. The average in two or more display cels extracted from two or more PDP(s) is shown in drawing 13 . Moreover, the case where a cel current is set as the case where it is set as 100 [muA], and 200 [muA] is shown. Moreover, aging time amount is for 1000 minutes. Moreover, 256 steps of on-duty is shown as zero to 255 level. r (r is integer of arbitration from 0 to 255) level corresponds to value (r/255) x (1/2566) of on-duty in case the pulse width of an aging control signal is r/255 of an one-line scan period. Therefore, 0 level is the case where aging actuation of the display cel is not carried out, and corresponds to the minimum value 0 of on-duty in case pulse width is 0. Moreover, 127 middle level corresponds to the on-duty values 1/512 in case pulse width is the one half of an one-line scan period at the maximums 1/256 of on-duty in case the pulse width of 255 level is an one-line scan period, respectively.

[0070] Only the aging-on time amount according to individual carries out aging actuation of each display cel, and it enabled it to adjust the I-V property of a display cel according to an individual in the gestalt 1 of the above-mentioned implementation by aging each display cel by common on-duty (it being 1/256, when there are 256 cathode lines) until the aging time amount set up according to the individual passes. However, when the aging time amount of all display cels is set as the same value, if on-duty is changed, the aging-on time amount of a display cel can be changed. At this time, a cel V intercept becomes small depending on on-duty, as shown in drawing 13 . Therefore, the I-V property of a display cel can be adjusted according to an individual also by aging each display cel by the on-duty according to individual. The aging approach of the gestalt 2 this operation is characterized by enabling it to amend the I-V property of a display cel according to an individual by aging until common aging time amount passes in the on-duty which the on-duty of each display cel was set [duty] up according to the individual, and had each display cel set up.

[0071] The configuration procedure of the individual on-duty of a display cel is the same as the configuration procedure of the individual aging time amount in the gestalt 1 of the above-mentioned implementation in general. However, it does not decide on aging time amount using the drop property of a cel V intercept over the aging time amount of drawing 9 like the gestalt 1 of the above-mentioned implementation, but the on-duty corresponding to the need decrement of a cel V intercept is decided using the cel V intercept drop property over the on-duty of drawing 13 .

[0072] Drawing 14 is drawing which plotted the setting-out on-duty of drawing 4 thru/or the display cel of drawing 7 in order of the scan. The case where it is the case where a setting-out cel current is 100 [muA], and 200 [muA] is shown in drawing 14 . The display cel whose setting-out on-duty is 0 level is a display cel which does not age.

[0073] On-duty is set up according to an individual for every display cel as mentioned above. Then, it ages by writing in the memory 83 (referring to drawing 11) of the aging equipment of the gestalt 2 of operation by making set-up on-duty into a cell data.

[0074] Thus, since dispersion between display cels of the cel current at the time of a constant voltage drive can be amended by aging each display cel of a panel by the on-duty according to individual, and having enabled it to adjust the I-V property of a display cel according to an individual according to the gestalt 2 of operation, a good pattern display without a non-LGT cel and an incorrect burning cel becomes possible.

[0075] In addition, in the gestalten 1 and 2 of the above-mentioned implementation, although aging of DC mold plasma display was explained, this invention can be equipped with two or more display cels of spontaneous light or non-spontaneous light, and can apply them also to a display (what has arranged the display cel to the single tier like line heads, such as a printer, is included) besides aging a display cel (or it being necessary to carry out).

[0076]

[Effect of the Invention] As explained above, it is effective in according to this invention, a good pattern display becoming possible since I-V property dispersion between display cels can be amended by only the aging-on time amount according to individual carrying out aging actuation of each display cel of a display, and having enabled it to adjust the I-V property of a display cel according to an individual.

[Translation done.]

【0076】

【発明の効果】以上説明したように本発明によれば、ディスプレイの各表示セルを個別のエージングオン時間だけエージング駆動し、表示セルのＩ－Ｖ特性を個別に調整できるようにしたことにより、表示セル間のＩ－Ｖ特性ばらつきを補正することができるので、良好なパターン表示が可能となるという効果がある。

【図面の簡単な説明】

【図１】本発明の実施の形態１のエージング装置の構成を示すブロック図である。

【図２】本発明の実施の形態１のエージング装置の構成を示す回路図である。

【図３】本発明の実施の形態１のエージング装置における駆動タイミングチャートである。

【図４】ＤＣ型プラズマディスプレイを定電流駆動したときの１陽極ラインに含まれる表示セルのセル電圧をプロットした図である。

【図５】図４に示した表示セルのセルインピーダンスをプロットした図である。

【図６】図４に示した表示セルのセルＶ切片をプロットした図である。

【図７】図４に示した表示セルを定電圧駆動するときのセル電流をプロットした図である。

【図８】図７のセル電流の度数分布図である。

【図９】任意の表示セルにおけるエージング時間に対するセルＶ切片の降下特性を示す図である。

【図１０】図４の表示セルの設定エージング時間をプロットした図である。

【図１１】本発明の実施の形態２のエージング装置の構成を示す回路ブロック図である。

【図１２】本発明の実施の形態２のエージング装置における駆動タイミングチャートである。

【図１３】任意の表示セルにおけるオンデューティに対するセルＶ切片の降下特性を示す図である。

【図１４】図４の表示セルの設定オンデューティをプロットした図である。

【図１５】ＤＣ型プラズマディスプレイの構造図である。

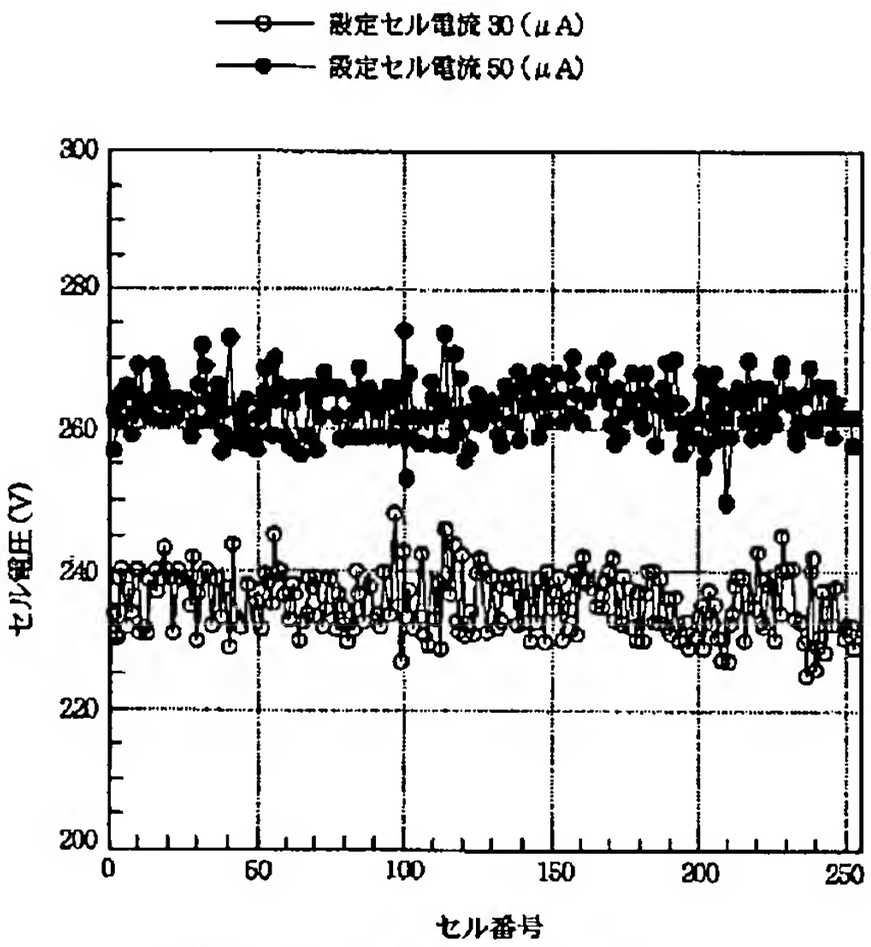
【図１６】従来のエージング装置の構成を示すブロック図である。

【図１７】従来のエージング装置における陽極定電流回路および陽極ドライバ回路の構成を示す回路ブロック図である。

【符号の説明】

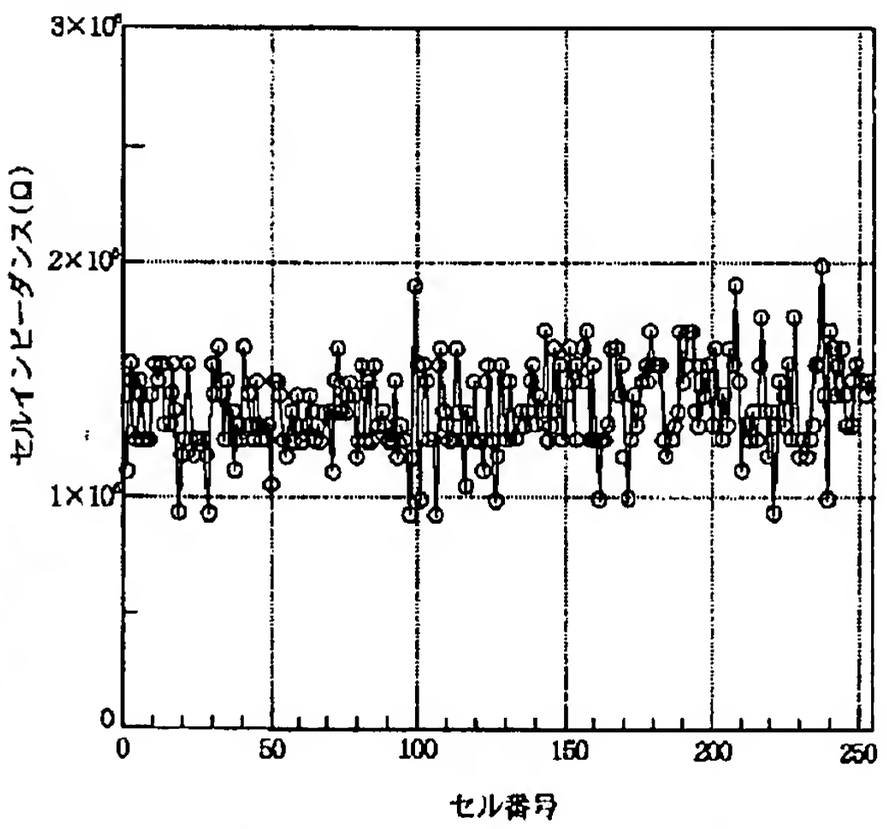
１　表示陽極定電流回路、　２　表示陽極ドライバ回路、　５　陰極ドライバ回路、　６，８　信号処理回路、　７　ＤＣ型プラズマディスプレイ、　２４陰極出力端子、　２５　表示陽極出力端子、　５１　シフトレジスタ、　６１，８１　基本信号発生回路、　６２，８２　アドレス信号発生回路、　６３　タイマ回路、　６４，６８　ラッチ回路、　６５，８３　メモリ、　６６　比較回路、　６７　シフトレジスタ回路、　Ｔｒ１～Ｔｒ５　トランジスタ、　Ｒ１，Ｒ２，Ｒ４，Ｒ５　抵抗、　Ｒｖ　ボリューム用可変抵抗。

【図4】



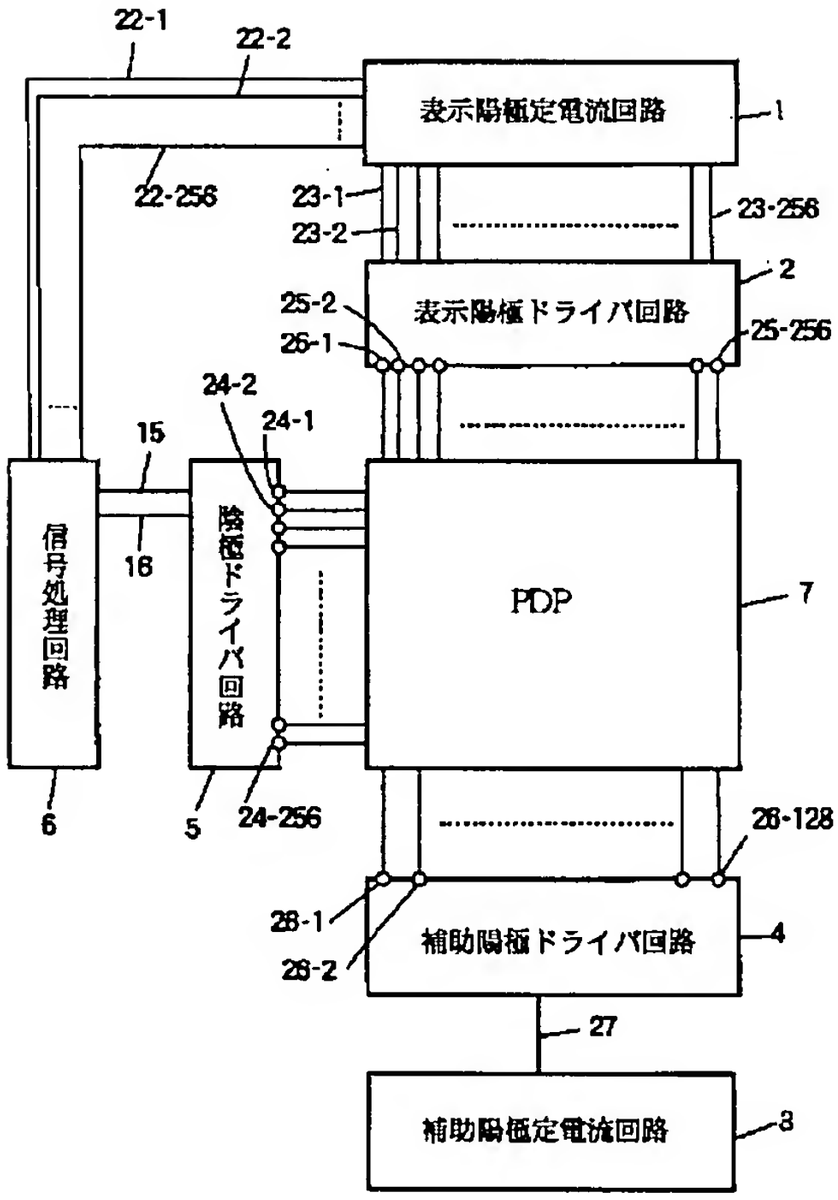
DC型PDPの1表示陽極ラインに含まれる表示セルの定電流駆動時セル電圧

【図5】

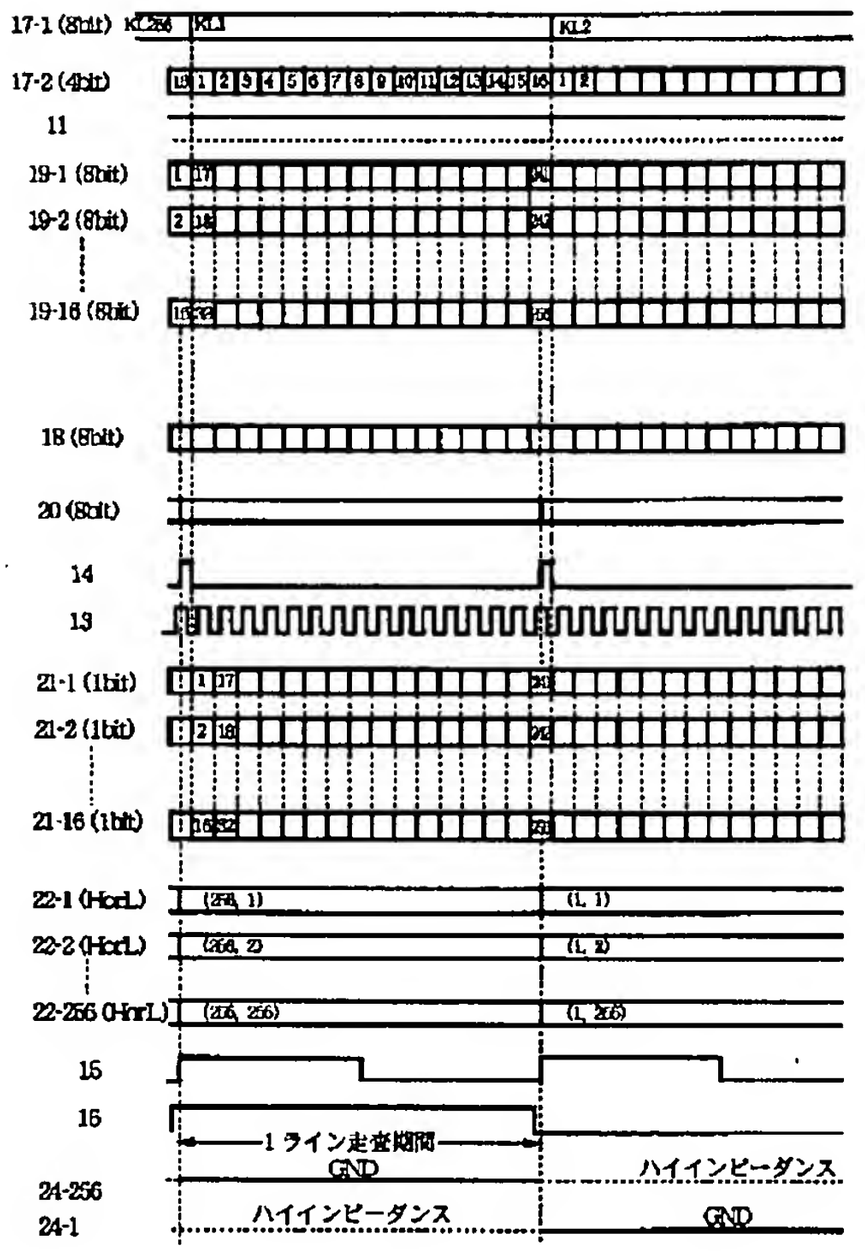


DC型PDPの1表示陽極ラインに含まれる表示セルのセルインピーダンス

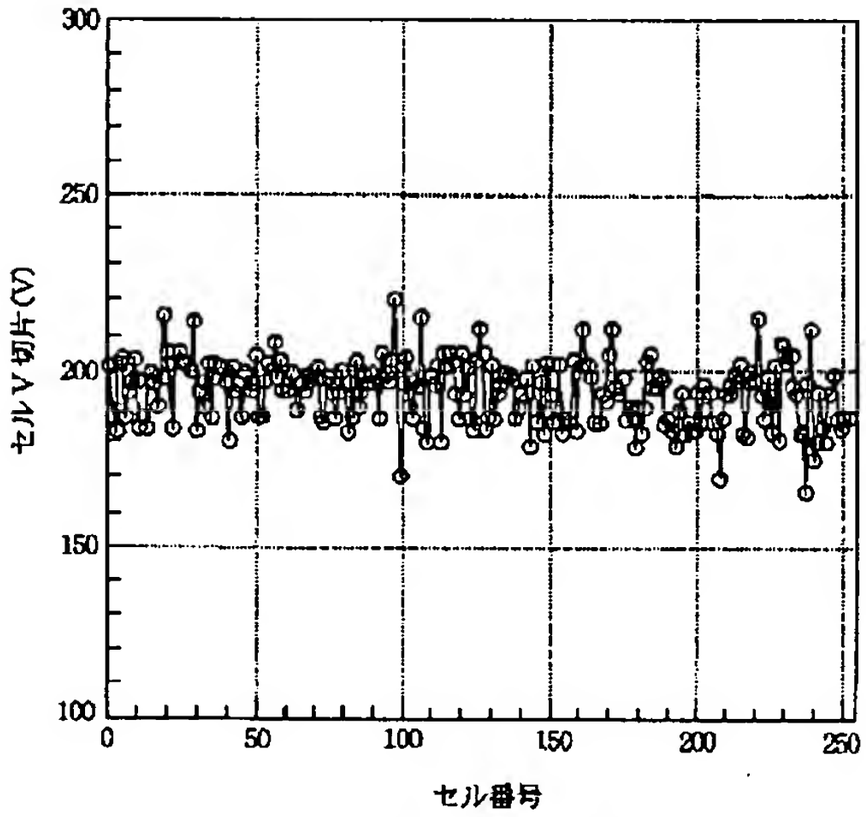
【図１】



【図３】

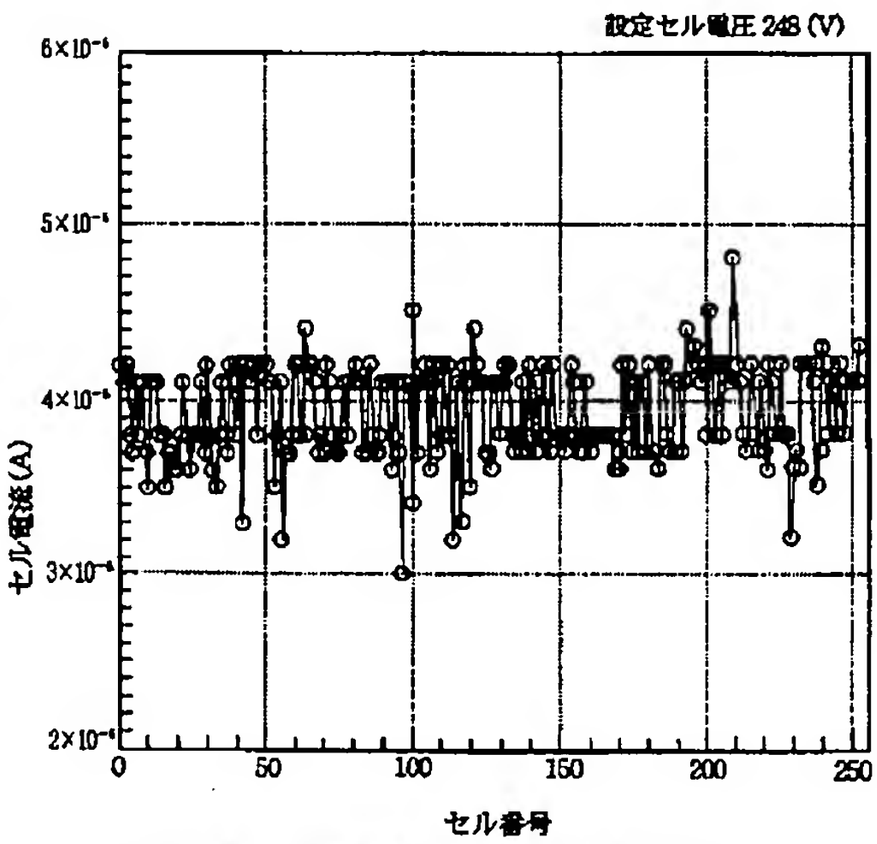


【図６】



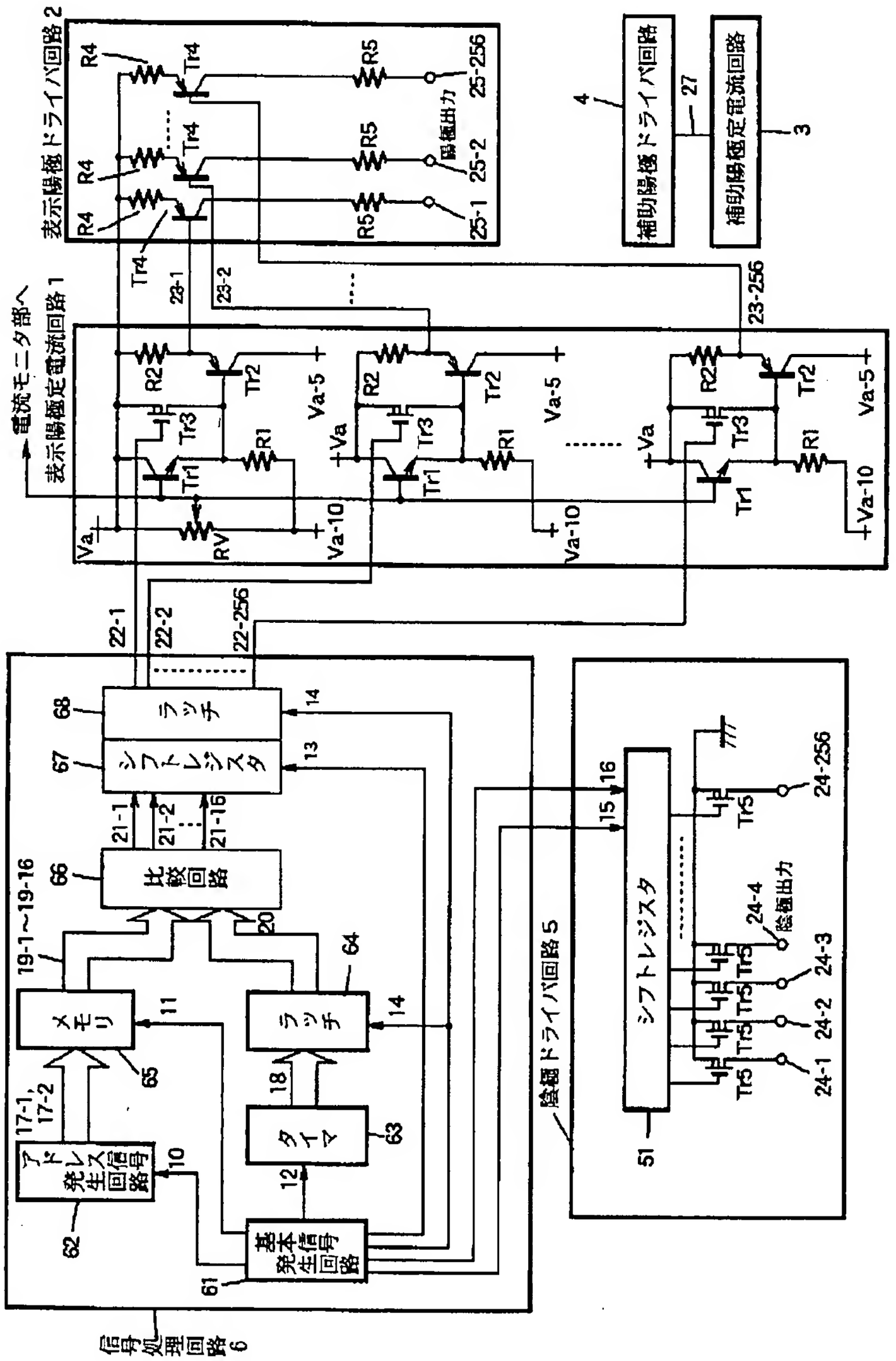
DC型PDPの１表示陽極ラインに含まれる表示セルのセルＶ切片

【図７】

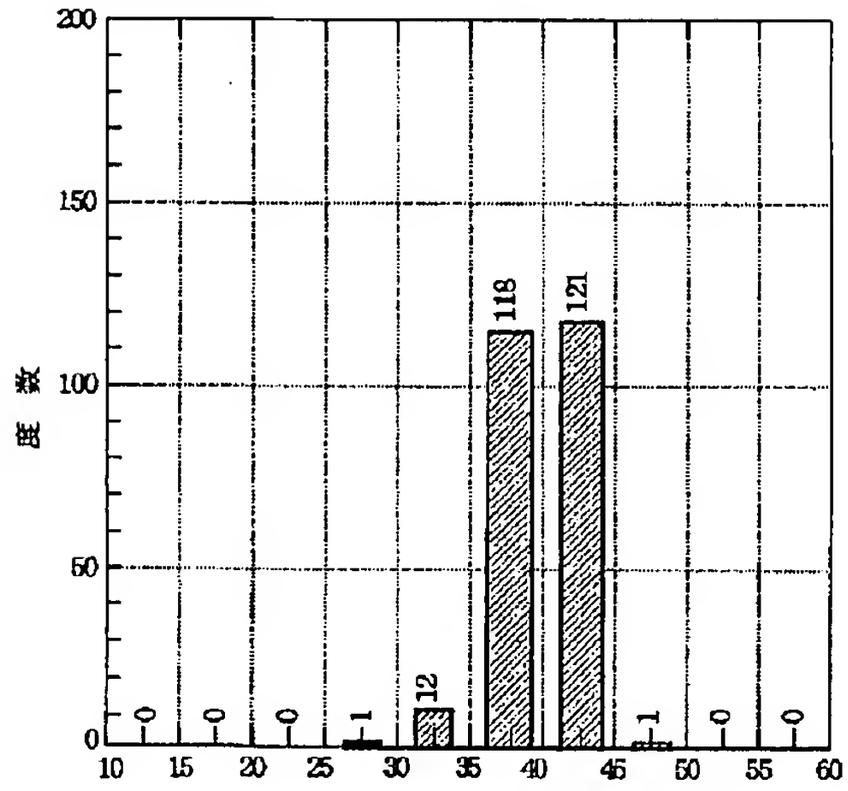


DC型PDPの１表示陽極ラインに含まれる表示セルの定電圧駆動時セル電流

【図2】

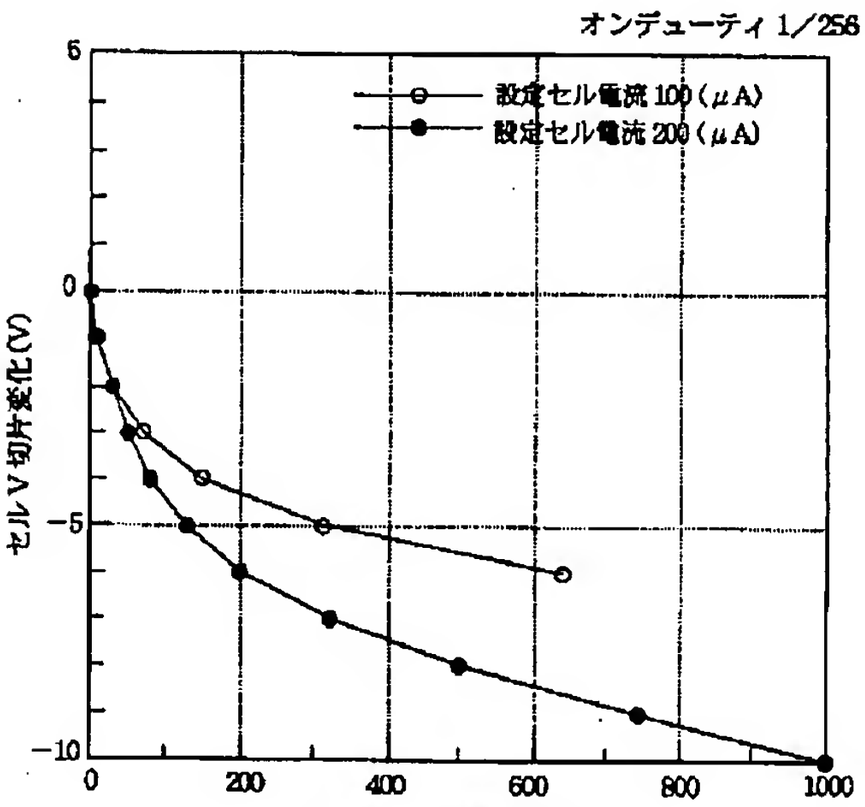


【図8】



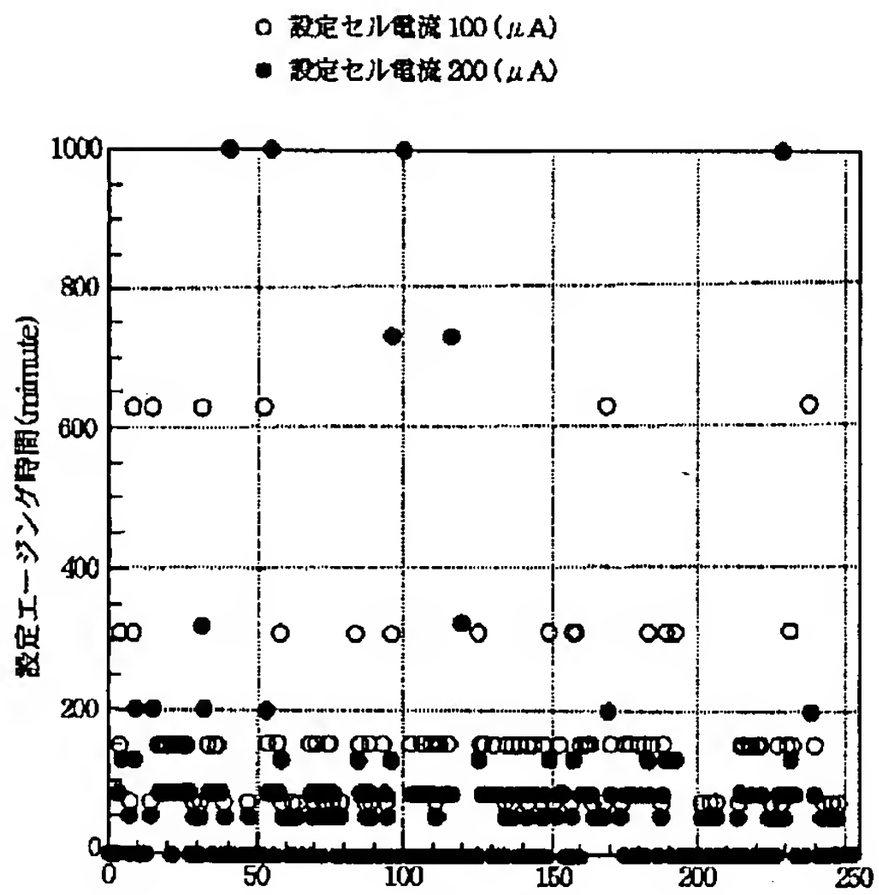
DC型PDPの1表示陽極に含まれる表示セルの定電圧駆動時セル電流の度数分布

【図9】



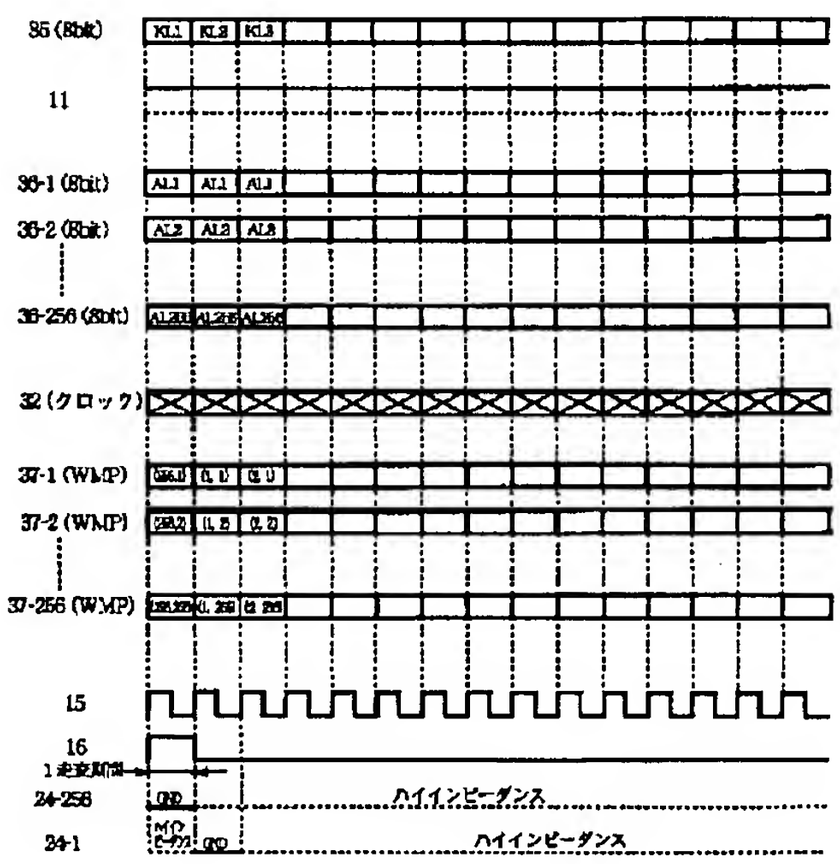
DC型PDPの表示セルのエージング時間に対するセルV切片変化

【図10】

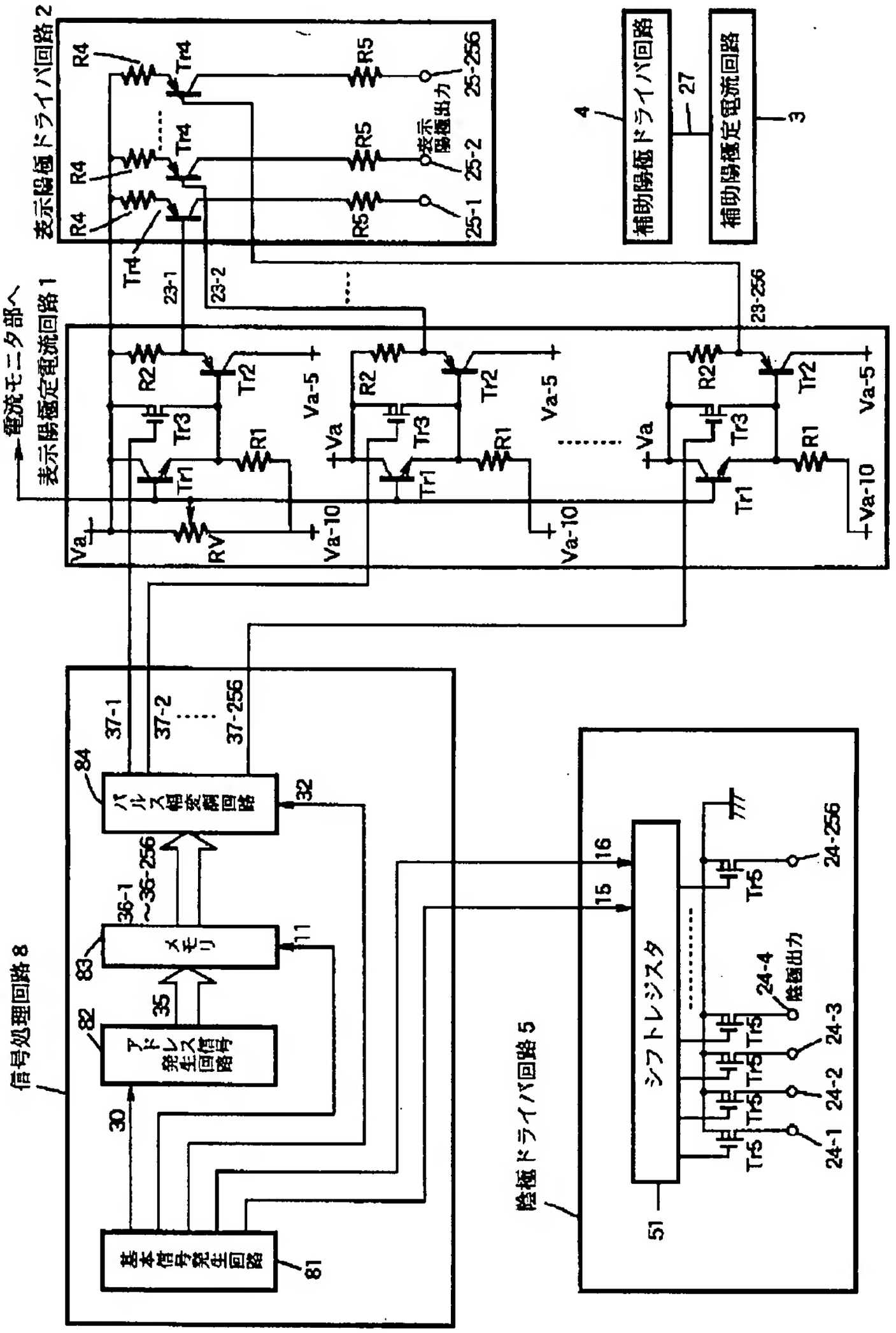


DC型PDPの1表示陽極ラインに含まれる表示セルのエージング時間設定値

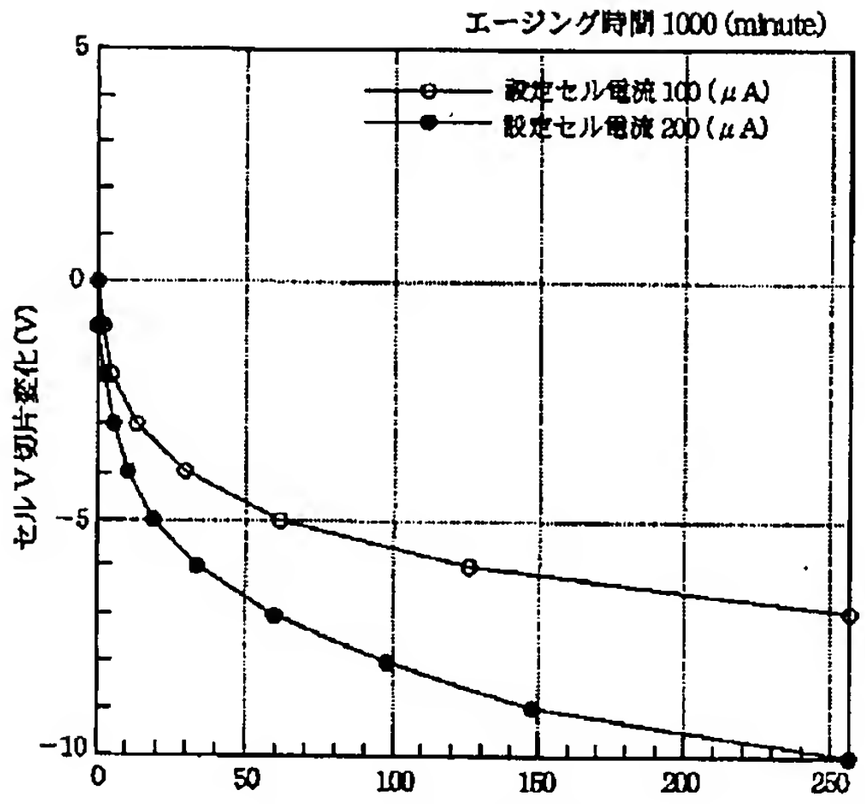
【図12】



【図11】

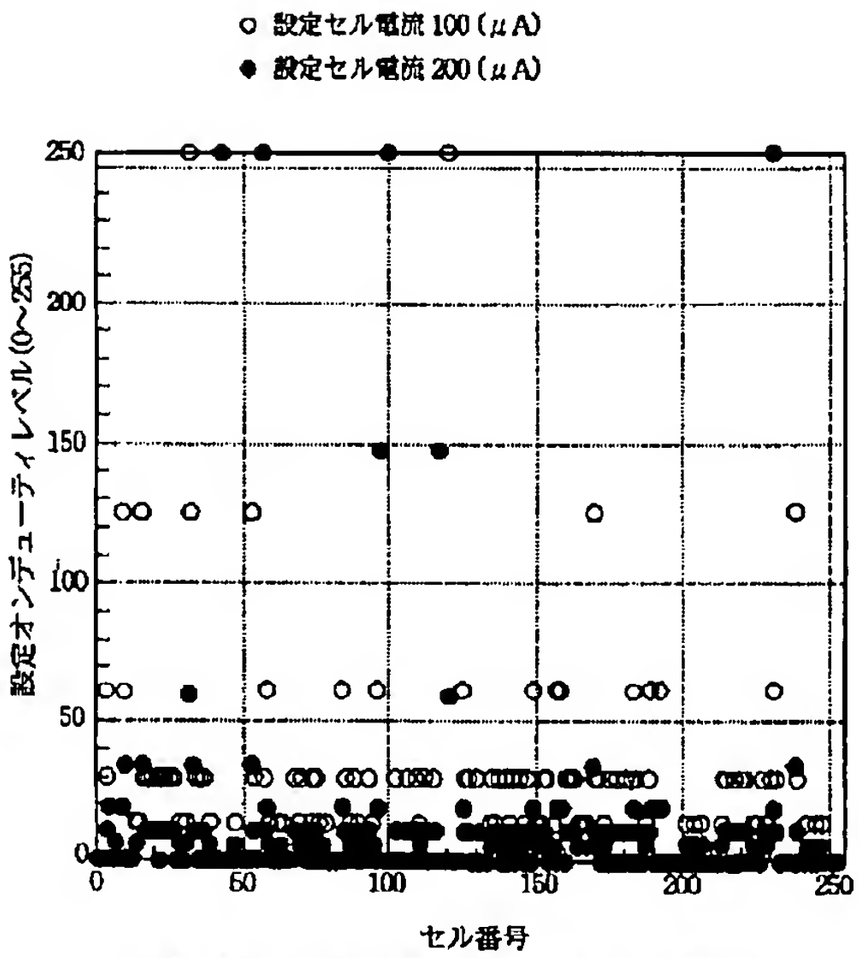


【図13】



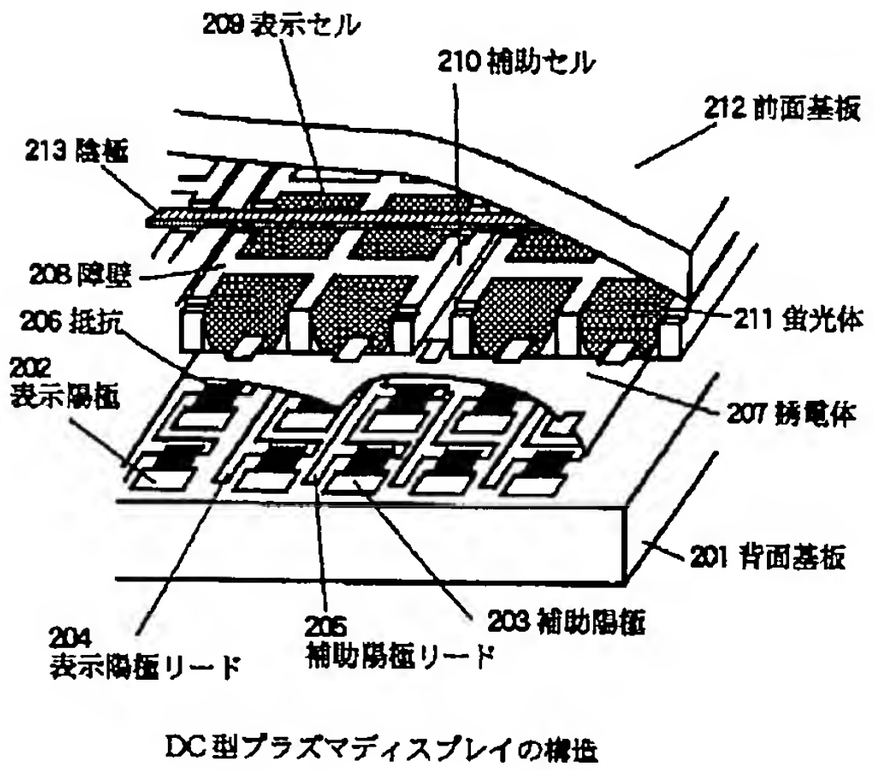
DC型PDPの表示セルのエージングオンデューティに対するセルV切片変化

【図14】



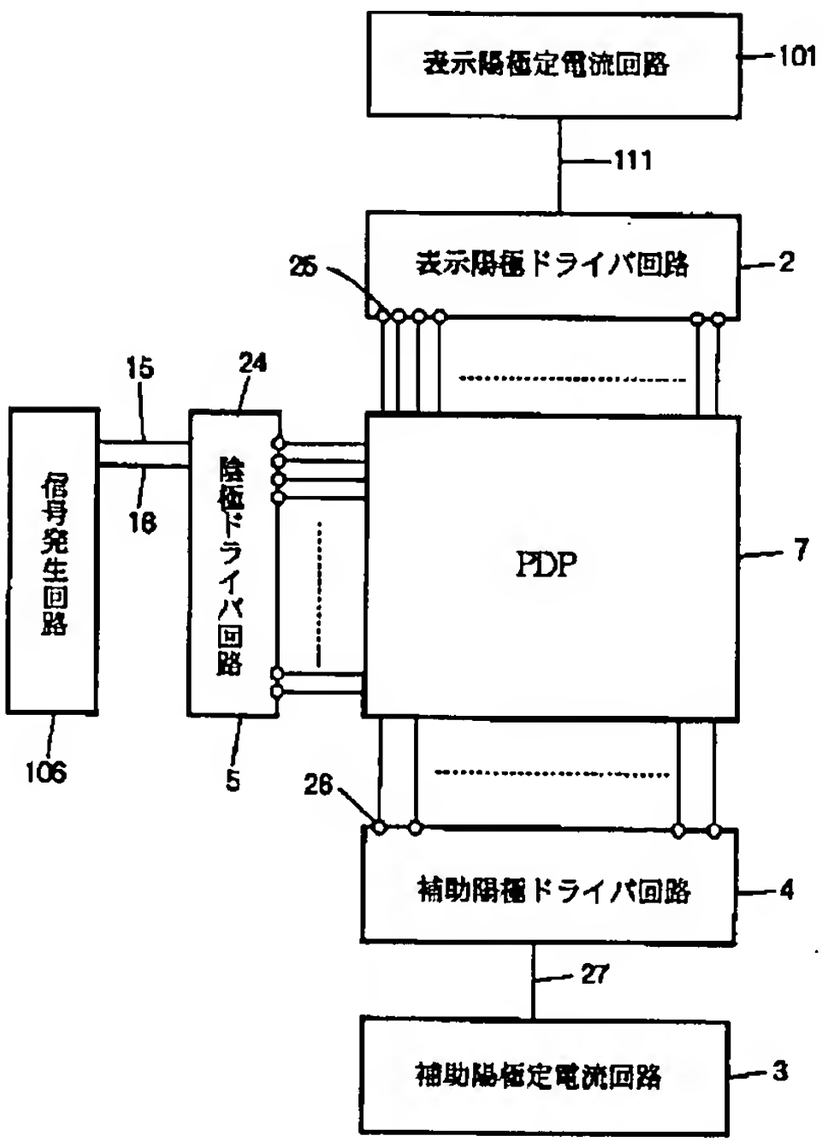
DC型PDPの1表示陽極ラインに含まれる表示セルのエージングオンデューティ設定値

【図15】



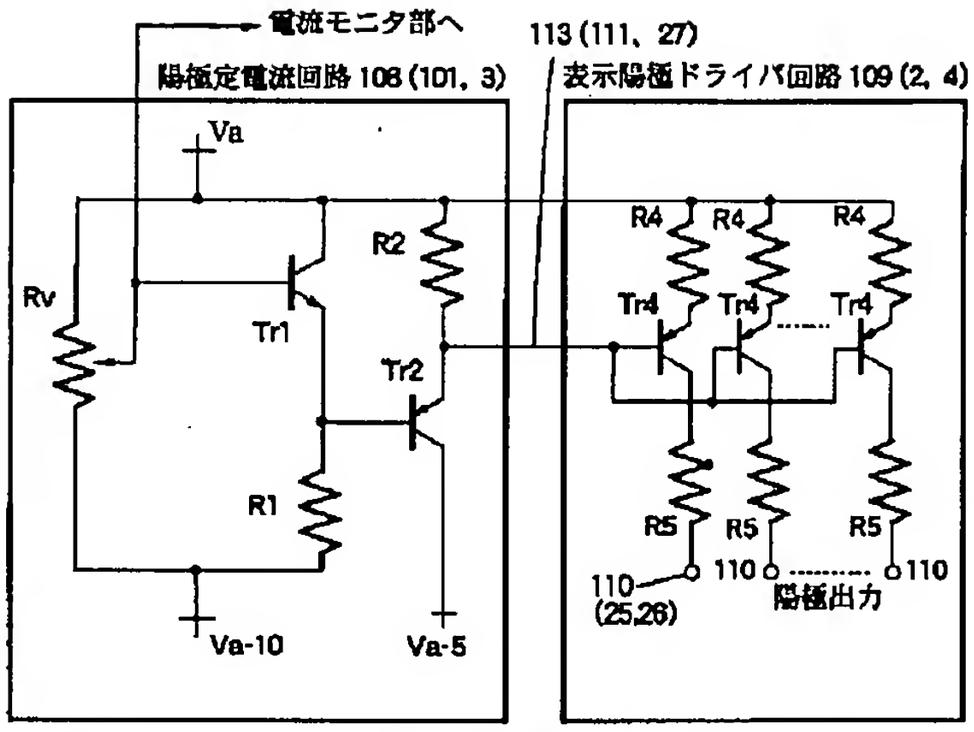
DC型プラズマディスプレイの構造

【図16】



従来のPDPエージング装置のブロック図

【図17】



従来のPDPエージング装置の陽極定電流回路及び陽極ドライバ回路

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